STHV748

Quad ± 90 V, ± 2 A, 3/5 levels, high speed ultrasound pulser

Datasheet — production data

QFN64 9 x 9 x1.0 mm

Features

- 0 to ±90 V output voltage
- Up to 20 MHz operating frequency
- Embedded low-power, floating high-voltage drivers (external voltage rails can be also used)
- Mode operations:
  - 3/5-levels output waveform
  - ±2 A source and sink current
  - Down ≤ 20 ps jitter
  - Anti-cross conduction function
  - Low 2nd harmonic distortion
- Fully integrated clamping-to-ground function
  - 8 Ω synchronous active clamp
  - Anti-leakage on output node
- Dedicated half bridge for continuous wave (CW) operations
  - ≤ 0.1 W power consumption
  - ±0.6 A source and sink current
  - 205 fs RMS jitter [100 Hz-20 kHz]
- Fully integrated T/R switch
  - 13.5 Ω on resistance
  - HV MOS topology to minimize current consumption
  - Up to 300 MHz BW
  - Receiver multiplexing function
- 2.4 V to 3.6 V CMOS logic interface
- Auxiliary integrated circuits
  - Noise blocking diodes
  - Fully self-biasing architecture
  - Anti-memory effect for all internal HV nodes
  - Thermal protection
  - Standby function
- Latch-up free due to HV SOI technology
- Very few external passive components needed

Applications

- Medical ultrasound imaging
- Pulse waveform generators
- NDT ultrasound transmission
- Piezoelectric transducer drivers

Description

This monolithic, high-voltage, high-speed pulser generator features four independent channels. It is designed for medical ultrasound imaging applications, but it can also be used for driving other piezoelectric, capacitive or MEMS based transducers. The STHV748 comprises a controller logic interface circuit, level translators, MOSFET gate drivers, noise blocking diodes, and high-power P-channel and N-channel MOSFETs as the output stage for each channel, clamping-to-ground circuitry, anti-leakage, anti-memory effect block, thermal sensor, and a T/R switch which guarantees an effective decoupling during the transmission phase. Moreover, the STHV748 includes self-biasing and thermal shutdown blocks. Each channel can support up to five active output levels with two half bridges. The output stage of each channel is able to provide ±2 A peak output current. In order to reduce power dissipation during continuous wave mode, a dedicated half bridge is available and the peak current is limited to 0.6 A.

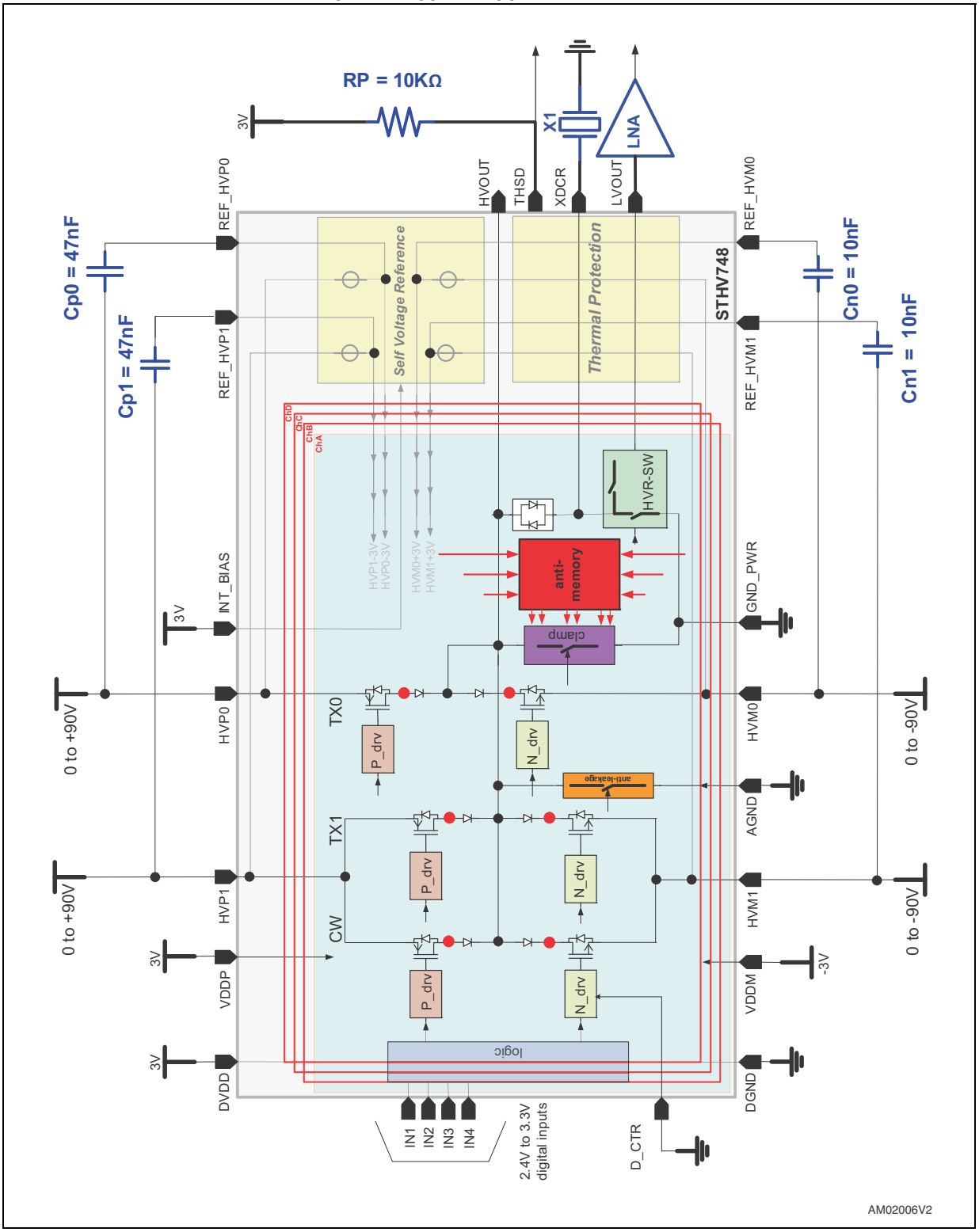
Table 1. Device summary

Order code	Package	Packaging
STHV748QTR	QFN64	Tape and reel

Contents

1 Typical application circuit

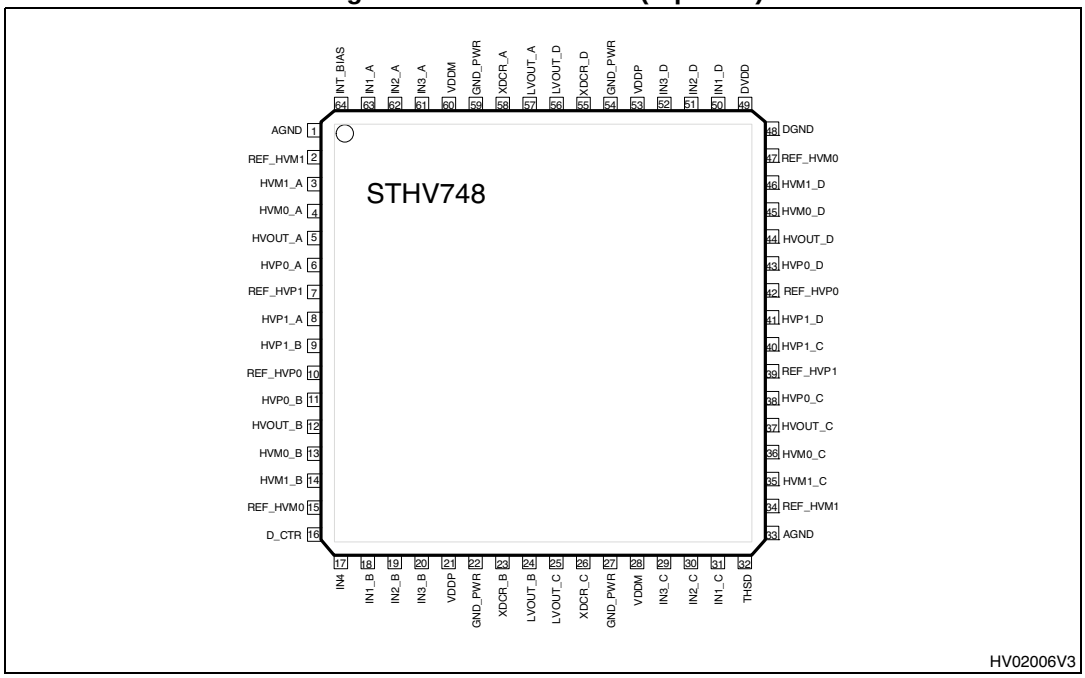
Figure 1. Typical application circuit



2 Pin settings

2.1 Connection

Figure 2. Pin connection (top view)



2.2 Description

Table 2. Pin description (P = power, A = analog, D = digital)

Pin N	Name	Function	IN/OUT	Type
1	AGND	Signal ground	I	A
2	REF_HVM1	Supply for low side 1 gate driver	I	P
3	HVM1_A	Negative high-voltage supply 1 channel A	I	P
4	HVM0_A	Negative high-voltage supply 0 channel A	I	P
5	HVOUT_A	Channel A, high-voltage output before noise blocking diodes	O	P
6	HVP0_A	Positive high-voltage supply 0 channel A	I	P
7	REF_HVP1	Supply for high side 1 gate driver	I	P
8	HVP1_A	Positive high-voltage supply 1 channel A	I	P
9	HVP1_B	Positive high-voltage supply 1 channel B	I	P
10	REF_HVP0	Supply for high side 0 gate driver	I	P
11	HVP0_B	Positive high-voltage supply 0 channel B	I	P

Table 2. Pin description (P = power, A = analog, D = digital) (continued)

Pin N	Name	Function	IN/OUT	Type
12	HVOUT_B	Channel B, high-voltage output before noise blocking diodes	O	P
13	HVM0_B	Negative high-voltage supply 0 channel B	I	P
14	HVM1_B	Negative high-voltage supply 1 channel B	I	P
15	REF_HVM0	Supply for low side 0 gate driver	I	P
16	D_CTR	Delay control	I	A
17	IN4	Input signal shared	I	D
18	IN1_B	Input signal channel B	I	D
19	IN2_B	Input signal channel B	I	D
20	IN3_B	Input signal channel B	I	D
21	VDDP	Positive low-voltage supply	I	A
22	GND_PWR	Power ground	I	P
23	XDCR_B	Channel B, high-voltage output	O	P
24	LVOUT_B	Channel B, low-voltage output	O	A
25	LVOUT_C	Channel C, low-voltage output	O	A
26	XDCR_C	Channel C, high-voltage output	O	P
27	GND_PWR	Power ground	I	P
28	VDDM	Negative low-voltage supply	I	A
29	IN3_C	Input signal channel C	I	D
30	IN2_C	Input signal channel C	I	D
31	IN1_C	Input signal channel C	I	D
32	THSD	Thermal shutdown pin	I/O	D
33	AGND	Signal ground	I	A
34	REF_HVM1	Supply for low side 1 gate driver	I	P
35	HVM1_C	Negative high-voltage supply 1 channel C	I	P
36	HVM0_C	Negative high-voltage supply 0 channel C	I	P
37	HVOUT_C	Channel C, high-voltage output before noise blocking diodes	O	P
38	HVP0_C	Positive high-voltage supply 0 channel C	I	P
39	REF_HVP1	Supply for high side 1 gate driver	I	P
40	HVP1_C	Positive high-voltage supply 1 channel C	I	P
41	HVP1_D	Positive high-voltage supply 1 channel D	I	P
42	REF_HVP0	Supply for high side 0 gate driver	I	P
43	HVP0_D	Positive high-voltage supply 0 channel D	I	P
44	HVOUT_D	Channel D, high-voltage output before noise blocking diodes	O	P

Table 2. Pin description (P = power, A = analog, D = digital) (continued)

Pin N	Name	Function	IN/OUT	Type
45	HVM0_D	Negative high-voltage supply 0 channel D	I	P
46	HVM1_D	Negative high-voltage supply 1 channel D	I	P
47	REF_HVM0	Supply for low side 0 gate driver	I	P
48	DGND	Logic ground	I	A
49	DVDD	Positive logic supply	I	A
50	IN1_D	Input signal channel D	I	D
51	IN2_D	Input signal channel D	I	D
52	IN3_D	Input signal channel D	I	D
53	VDDP	Positive low-voltage supply	I	A
54	GND_PWR	Power ground	I	P
55	XDCR_D	Channel D, high-voltage output	O	P
56	LVOUT_D	Channel D, low-voltage output	O	A
57	LVOUT_A	Channel A, low-voltage output	O	A
58	XDCR_A	Channel A, high-voltage output	O	P
59	GND_PWR	Power ground	I	P
60	VDDM	Negative low-voltage supply	I	A
61	IN3_A	Input signal channel A	I	D
62	IN2_A	Input signal channel A	I	D
63	IN1_A	Input signal channel A	I	D
64	INT_BIAS	Enable internal supply generators	I	D
Exposed-Pad		Substrate	I	P

2.3 Additional pin description

The INT_BIAS pin enables the internal reference generators. With INT_BIAS=DVDD, the STHV748 internally generates the reference voltages on REF_HVP1/0 (pin - 7, 10, 39, 42) and REF_HVM1/0 (pin - 2, 15, 34, 47). These voltages are set at VDDP below HVP and respectively at:

- REF_HVM# = HVM# + VDDP
- REF_HVP# = HVP# - VDDP

After enabling INT_BIAS, a period of time is needed to charge the external reference capacitors (about 30 µs in a typical application).

Should INT_BIAS=DGND, it is necessary to apply an external voltage reference to the REF_HVM# and REF_HVP# pins.

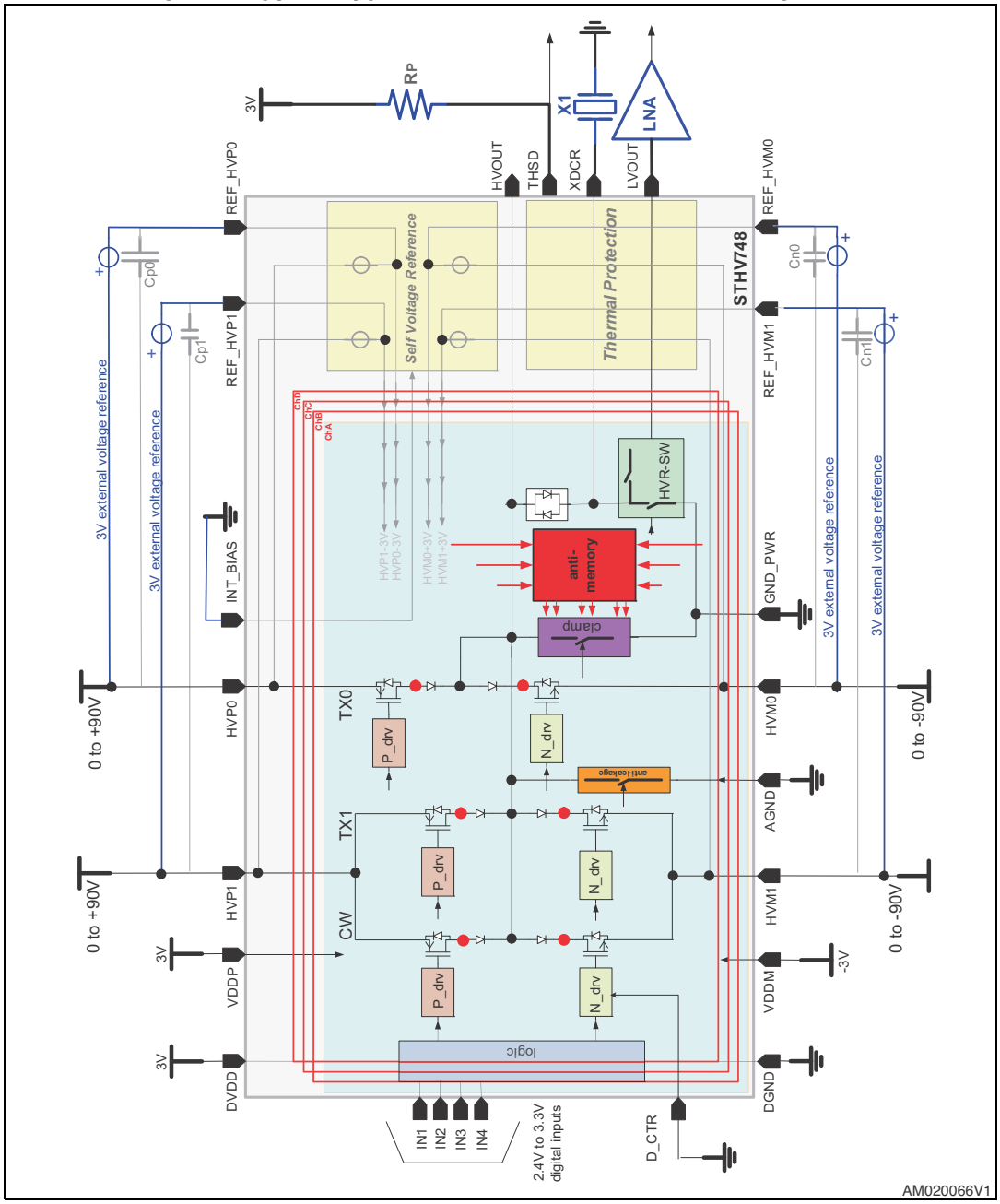
THSD is a thermal flag. Being the output stage of the THSD a Nch-MOS open-drain, an external pull-up resist or (Rp≥10 kΩ) connected to a positive low-voltage supply (see *Figure 1*) is required. If the internal temperature surpasses 153 °C, THSD goes down and all STHV748 channels are in HZ state. The thermal protection can be disabled, by connecting

the THSD pin to a positive low voltage supply. THSD can be also shared among several STHV748 on the same PCB.

D_CTR can be used to optimize 2nd HD performances by tuning the fall propagation delay (tdf - see *Table 9*). If D_CTR is equal to ground, tdf has the nominal value. If D_CTR is varied from 2 V to 4.2 V, tdf can be changed from -1 ns to +600 ps with respect to the nominal value.

The exposed-pad is internally connected to the substrate of the package. It can be either left floating or connected to a ground via 100 V capacitance toward ground, in order to reduce the noise during the receiving phase.

Figure 3. Typical application with INT_BIAS shorted to ground



3 Truth table and single channel block description

Figure 4. Single channel block description

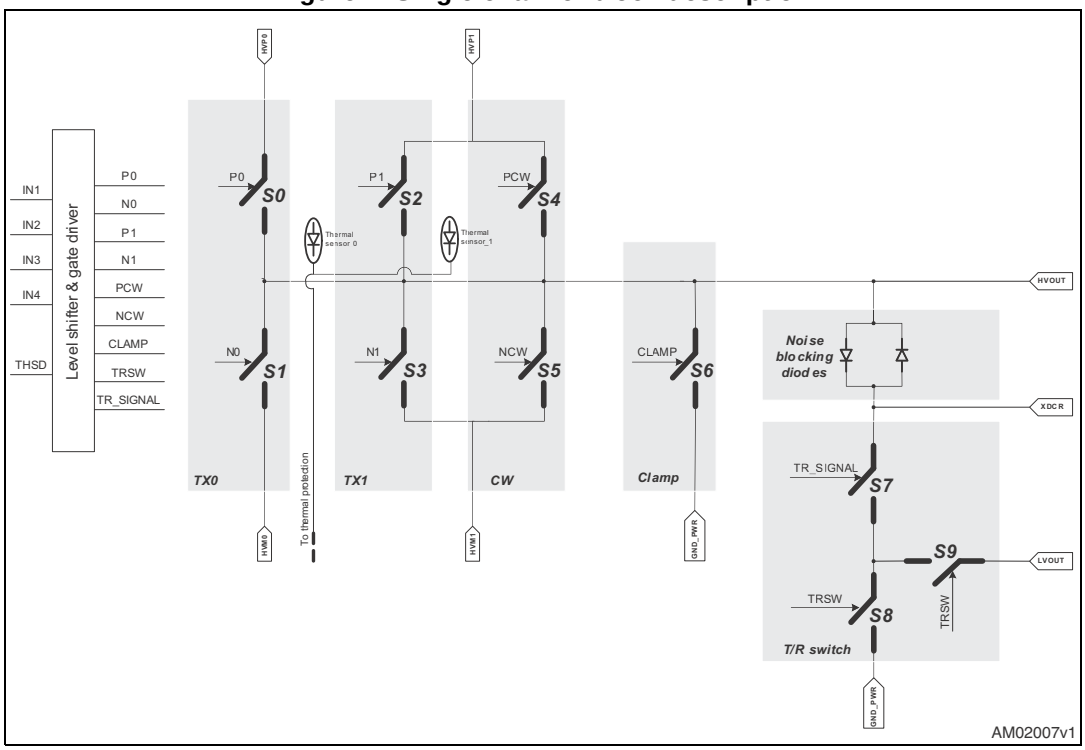


Table 3. Truth table for one channel

Global		Per channel			State	Switches internal state									
THSD	IN4	IN3	IN2	IN1		S0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	x	x	0	0	Clamp	0	0	0	0	0	0	1	0	1	0
1	0	0	0	1	HVM0	0	1	0	0	0	0	0	0	1	0
1	0	0	1	0	HVP0	1	0	0	0	0	0	0	0	1	0
1	x	0	1	1	T/R SW	0	0	0	0	0	0	1	1	0	1
1	0	1	0	1	HVM1	0	0	0	1	0	0	0	0	1	0
1	0	1	1	0	HVP1	0	0	1	0	0	0	0	0	1	0
1	0	1	1	1	HZ	0	0	0	0	0	0	0	0	1	0
1	1	1	1	1	T/R SW	0	0	0	0	0	0	1	1	0	1
1	1	0	0	1	Max. HVM0 and HVM1	0	1	0	1	0	0	0	0	1	0
1	1	0	1	0	Max. HVP0 and HVP1	1	0	1	0	0	0	0	0	1	0
1	1	1	0	1	CW HVM1	0	0	0	0	0	1	0	0	1	0
1	1	1	1	0	CW HVP1	0	0	0	0	1	0	0	0	1	0
0	x	x	x	x	HZ	0	0	0	0	0	0	0	0	1	0

4 Power-up / Power-down voltage sequence

During the power up/power down phases, the following relationship must be always respected:

- VDDP >= DVDD
- HVM0 <= HVM1
- HVP0 >= HVP1

It is recommended to power up the low voltage supplies before the high voltage supplies.

5 Electrical data

5.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AGND	Analog ground reference (1)	0	V
DGND	Digital ground	-300 to 300	mV
GND_PWR	Power ground	-1.2 to 1.2	V
VDDP	Positive supply voltage	-0.3 to 3.9	V
VDDM	Negative supply voltage	0.3 to -3.9	V
DVDD	Positive logic voltage	-0.3 to VDDP	V
HVP0	TX0 high-voltage positive supply	95	V
HVP1	TX1 high-voltage positive supply	0 to HVP0	V
HVM0	TX0 high-voltage negative supply	-95	V
HVM1	TX1 high-voltage negative supply	0 to HVM0	V
REF_HVP#	High-voltage positive gate supply	-0.3 < HVP - REF_HVP < 3.6	V
REF_HVM#	High-voltage negative gate supply	-0.3 < REF_HVM - HVM < 3.6	V
XDCR	High-voltage output	-95 to 95	V
HVOUT	High-voltage output before noise blocking diodes	-95 to 95	V
LVOUT	Low-voltage output	-1 to 1	V
DIG I/O	Digital input specified in *Table 2*	-0.3 to DVDD + 0.3	V
D_CTR	Delay control	-0.3 to 4.6	V
T_{OP}	Operating temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C

1. AGND is the ground reference for all the other voltages.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th,JA}$	Thermal resistance junction-ambient	30 (1)	°C/W

1. This value is given for a two layer PCB (2S2P) and it's strongly sensitive to PCB layout. Increasing the number of PCB layers and/or adding heat sinks vias, the thermal resistance value decreases.

6 Operating supply voltages and average currents

Operating conditions, unless otherwise specified, only ONE channel on, no load, HV=90 V, TX0 and TX1 on, INT_BIAS=DVDD, DVDD=3 V, VDDP=3 V and VDDM=-3 V

Table 6. Supply voltages and average currents

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDDP	Positive supply voltage		2.7	3	3.6	V
I_{VDDP}	Positive supply current	PW mode (1)			1.5	mA
I_{VDDP_Q}		Standby mode (2)		1.1		mA
VDDM	Negative supply voltage		-2.7	-3	-3.6	V
I_{VDDM}	Negative supply current	PW mode	-1.5			mA
I_{VDDM_Q}		Standby mode		-800		µA
DVDD	Positive logic voltage		2.4	3	min(3.6,V DDP+0.3)	V
$I_{\_DVD}$	Logic supply current	PW mode			100	µA
$I_{\_DVD\_Q}$		Standby mode			85	µA
HVP	High-voltage positive supply		0		90	V
I_{HVP}	HV positive supply current	PW mode			1	mA
I_{HVP_Q}		Standby mode			350	µA
HVM	High-voltage negative supply		-90		0	V
I_{HVM}	HV negative supply current	PW mode	-1			mA
I_{HVM_Q}		Standby mode	-350			µA
HVP-REF_HVP	High-voltage positive gate supply		2.7	3	3.6	V
REF_HVM-HVM	High-voltage negative gate supply		2.7	3	3.6	V
D_CTR	Delay control		0		4.2	V

1. In PW pulse wave mode the average current is measured over $T_{\_w\ time}$ (see *Figure 6*).
2. In standby mode all channels are in HZ and INT_BIAS= AGND

6.1 Digital inputs

Table 7. Digital inputs

Symbol	Parameter	Min.	Max.	Units
IN1_#, IN2_#, IN3_#, IN4, INT_BIAS, THSD	Input logic high-voltage	0.8 DVDD	DVDD	V
IN1_#, IN2_#, IN3_#, IN4, INT_BIAS, THSD	Input logic low-voltage	0	0.2 DVDD	V

6.2 Output signals

Table 8. Output signals

Symbol	Parameter	Min.	Max.	Units
HVOUT	High-voltage output before noise blocking diodes	-90	90	V
XDCR	High-voltage output	-90	90	V
LVOUT	Low-voltage output	-1	1	V
THSD	Thermal shutdown pin	0	3	V

7 Electrical characteristics

Table 9. Static electrical characteristics (1)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_N	Saturation current S1 - S3	HVP# =10 V, HVM# =-10 V, HVOUT=0 V	1.1	1.30		A
		HVP# =25 V, HVM# =-25 V, HVOUT=0 V		1.70		A
		HVP# =90 V, HVM# =-90 V, HVOUT=0 V		2		A
I_P	Saturation current S0 - S2	HVP# =10 V, HVM# =-10 V, HVOUT=0 V	1	1.30		A
		HVP# =25 V, HVM# =-25 V, HVOUT=0 V		1.70		A
		HVP# =90 V, HVM# =-90 V, HVOUT=0 V		2		A
I_{NCW}	Saturation current S5	HVP1=10 V, HVM1=-10 V, HVOUT=0 V	300	350		mA
I_{PCW}	Saturation current S4	HVP1=10 V, HVM1=-10 V, HVOUT=0 V	390	480		mA
I_{CL}	Saturation current S6	HVOUT=25 V		1.5		A
R_{ON_CLAMP}	On resistance S6	HVOUT=1 V		8		W
I_L	Output leakage current, per channel	HVP# = 90 V, HVM# = -90 V, HVOUT=0 V		1		µA
		HVP# = 90 V, HVM# = -90 V, HVOUT=-90 V		1		
		HVP# = 90 V, HVM# = -90 V, HVOUT=+90 V		1		
P_{SB}	Power dissipation in standby mode	HVP# = 90 V, HVM# = -90 V, HVOUT=0 V, INT_BIAS=DGND		4		µW
		HVP# = 90 V, HVM# = -90 V, HVOUT=0 V		126	150	mW
P_{RX}	Power dissipation in HVR_SW state	HVP# = 30 V, HVM# = -30 V, INT_BIAS =0, all channels in receiving phase		30		mW
V_{REFP}	HVP# - REF_HVP#	HVP# = 10 V, HVM# = -10 V, HVOUT=0 V	0.8 VDDP		1.2 VDDP	V
V_{REFN}	REF_HVM# - HVM#	HVP# = 10 V, HVM# = -10 V, HVOUT=0 V	0.8 VDDP		1.2 VDDP	V
T_{OTP}(2)	Overtemperature threshold	HVP# =10 V, HVM# =-10 V	130	153	160	°C
T_{HYS}	OTP hysteresis	HVP# =10 V, HVM# =-10 V		40		°C

Table 9. Static electrical characteristics (1) (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$C_{T/R\ SW}$	T/R SW capacitance	LVOUT=0 V		40		pF
$R_{T/R\ SW\_ON}$	T/R SW on resistance	HVP# =10 V, HVM# =-10 V, XDCR=0 V, LVOUT=0.2 V		13.5	15.5	W
$R_{T/R\ SW\_OFF}$	T/R SW off resistance	HVP# =10 V, HVM# =-10 V, XDCR=1 V, LVOUT=0 V	1			GΩ
VDROP_CW	Voltage drop between HVP1 and XDCR	HVP# =10V, HVM# =-10V, I_{SINK_XDCR}=50 mA	2.58	2.79	2.9	V
	Voltage drop between XDCR and HVM1	HVP# =10V, HVM# =-10V, I_{SOURCE_XDCR}=50 mA	2.58	2.86	2.9	V

1. Operating conditions, unless otherwise specified, INT_BIAS=DVDD, HVP# = 90 V, HVM# = -90 V, VDDP = 3 V, VDDM = -3 V, DVDD = 3 V, TROOM = 25 °C.
2. Guaranteed by bench characterization.

Table 10. AC electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
f	Maximum output frequency		16			MHz
		50 pF//200 Ω		22		MHz
f_{CW}	Maximum output frequency CW	HVP1 =5 V, HVM1 = -5 V, continuous wave mode		20		MHz
f_{BW}	Output frequency BW	HVP1 = 50 V, HVM1 = -50 V, continuous wave mode, 50 pF//200 Ω		10		MHz
$t_{j\text{-}CW}$	CW output jitter	HVP1 =5 V, HVM1 = -5 V, continuous wave mode		205		fs, rms
t_f	Fall time			28		ns
t_r	Rise time			28		ns
t_{dr}	Rise propagation delay			24		ns
t_{df}	Fall propagation delay			24		ns
T/R SW	T/R SW turn-on / turn-off time			170		ns
HD2	2^{nd} harmonic distortion	1 pulse f = 1.7 MHz		-40		dBc
		1 pulse f = 5 MHz		-40		dBc
		5 pulses f = 1.7 MHz		-40		dBc
		5 pulses f = 5 MHz		-40		dBc
HD2PC	Pulse cancellation	f = 1.7 MHz original and inverted pulse		-40		dBc
		f = 5 MHz original and inverted pulse		-40		dBc
BVD	Burst voltage drop	1^{st} to 128^{th} pulse HVP1 = 10 V, HVM1 = -10 V		2		%

Table 10. AC electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Units
P_{D_CW}	Power dissipation, all channels	CW mode, f = 5 MHz, HVP1 = 5 V, HVM1 = -5 V, no load		390		mW
	Power dissipation, one channel	CW mode, f = 5 MHz, HVP1 = 5 V, HVM1 = -5 V			320	
T/R SW_{SPIKE}	T/R SW spike on XDCR and LVOUT			100		mV_{pp}
X_{TALK}	Cross talk between channels.	Ampl(2ch)/Ampl(1ch), 50 pF//200 Ω		-40		db

1. Operating conditions, unless otherwise specified, HVP# = 90 V, HVM# = -90 V, VDDP = 3 V, VDDM = -3 V, DVDD = 3 V, V, INT_BIAS = DVDD, (HVP-REF_HVP) = 3 V, (REF_HVM-HVM) = 3 V, XDCR load C = 300 pF//R = 100 Ω, LVOUT load C = 20 pF//200 Ω T_{ROOM} = 25 °C.

8 Timings

Figure 5. t_r, t_f, t_{dr}, and t_{df} descriptions

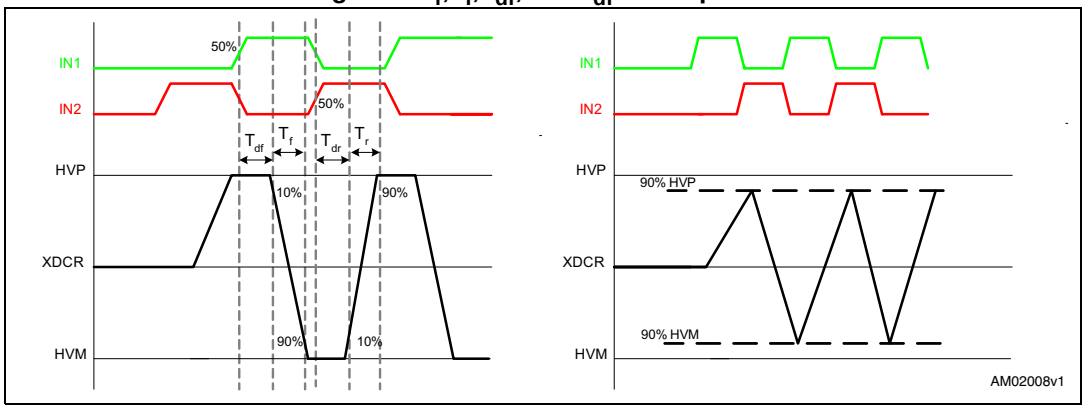


Figure 6. PW example 5 periods, HVP0 = 90 V, HVM0 = -90 V, T=200 ns, T_tx=1.2 µs, T_w=200 µs

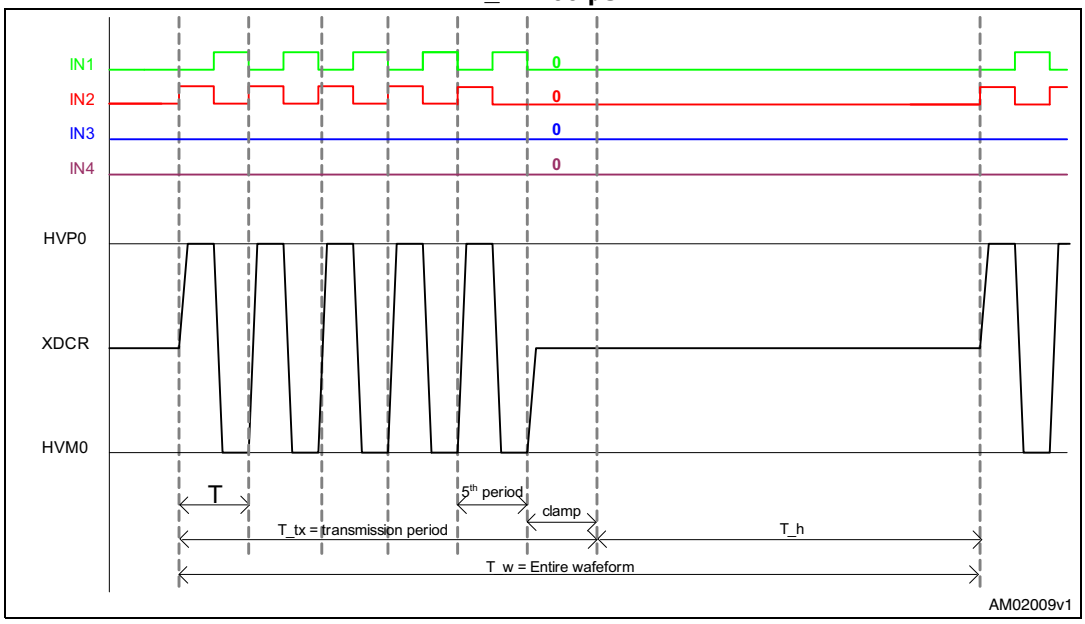


Figure 7. PW and HD2 example (HVP0=80 V, HVM0=-80 V load 300 pF//100 Ω)

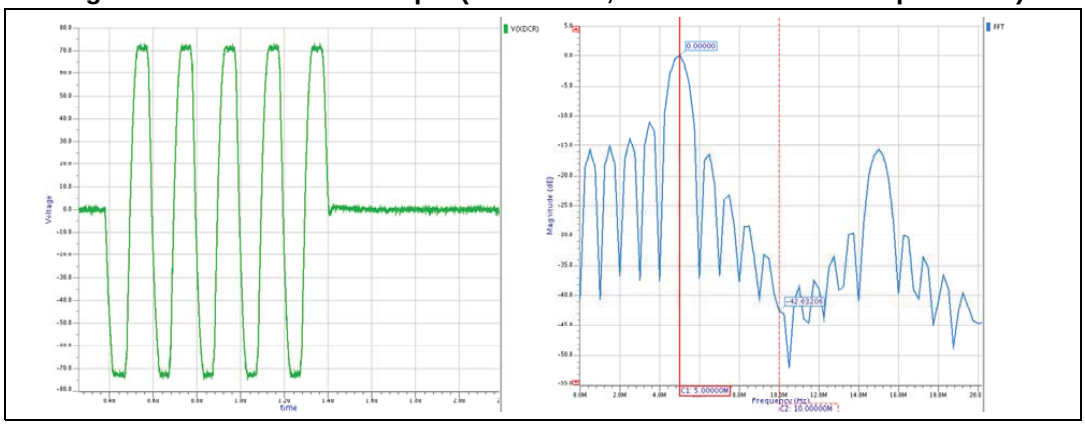


Figure 8. PC example, HVP0 = 90 V HVM0 = -90 V, T=200 ns, T_pos= T_neg=400 ns

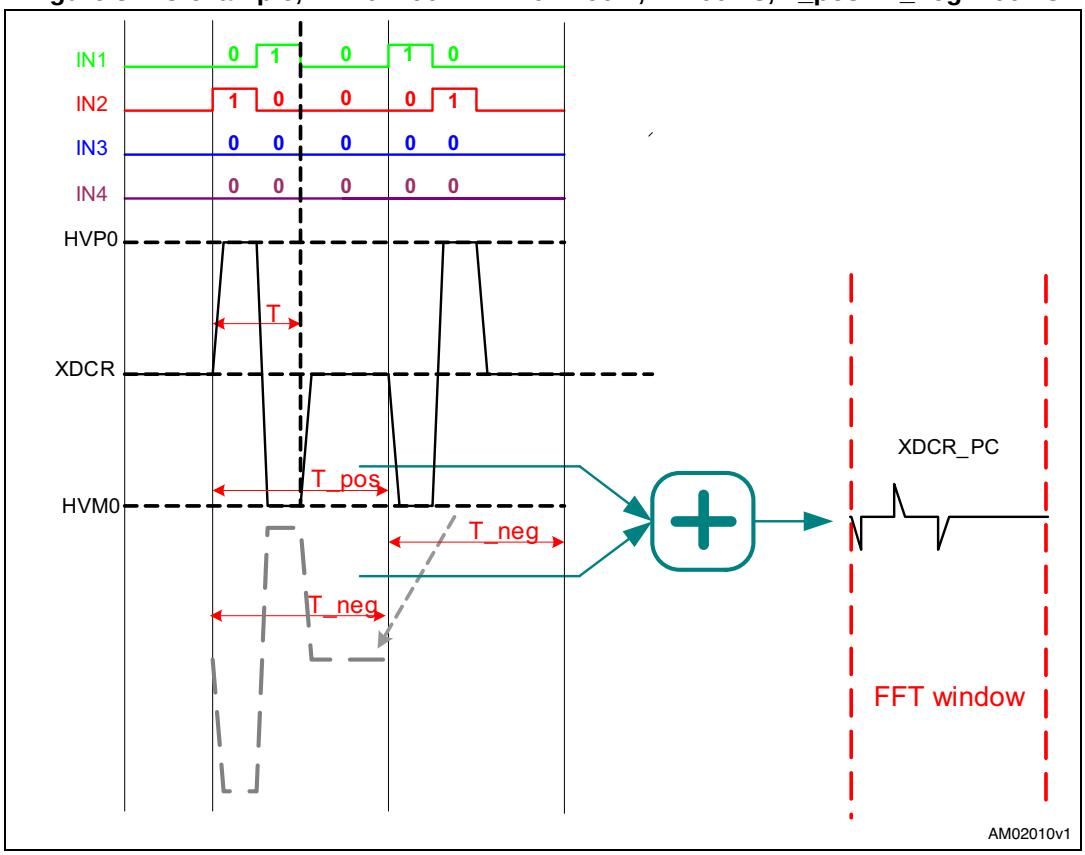


Figure 9. CW mode example, HVP1 = 5 V, HVM1 = 5 V, T = 200 ns, T_tx>1 ms

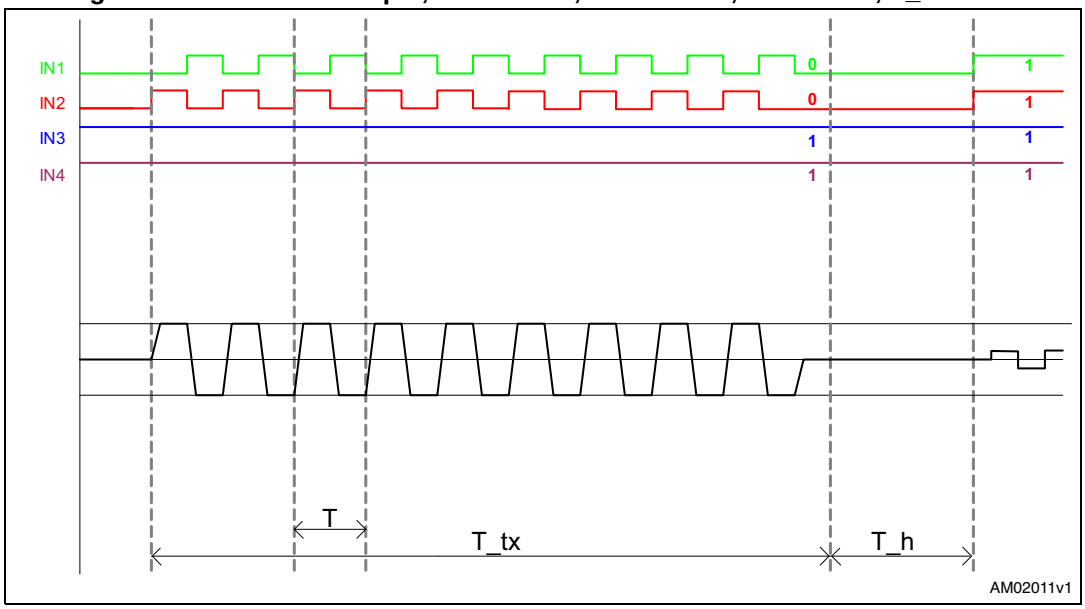


Figure 10. T/R SW signal equivalent circuit model

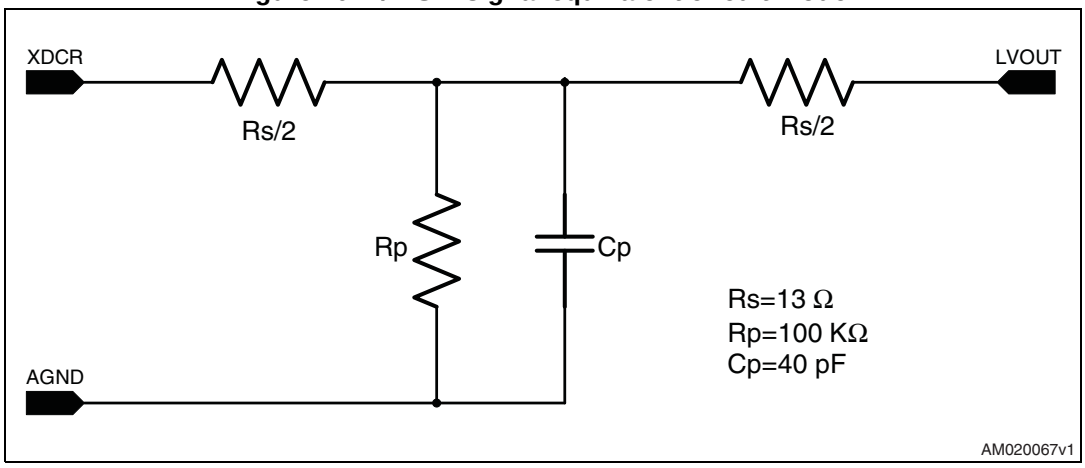


Figure 11. T/R SW bandwidth

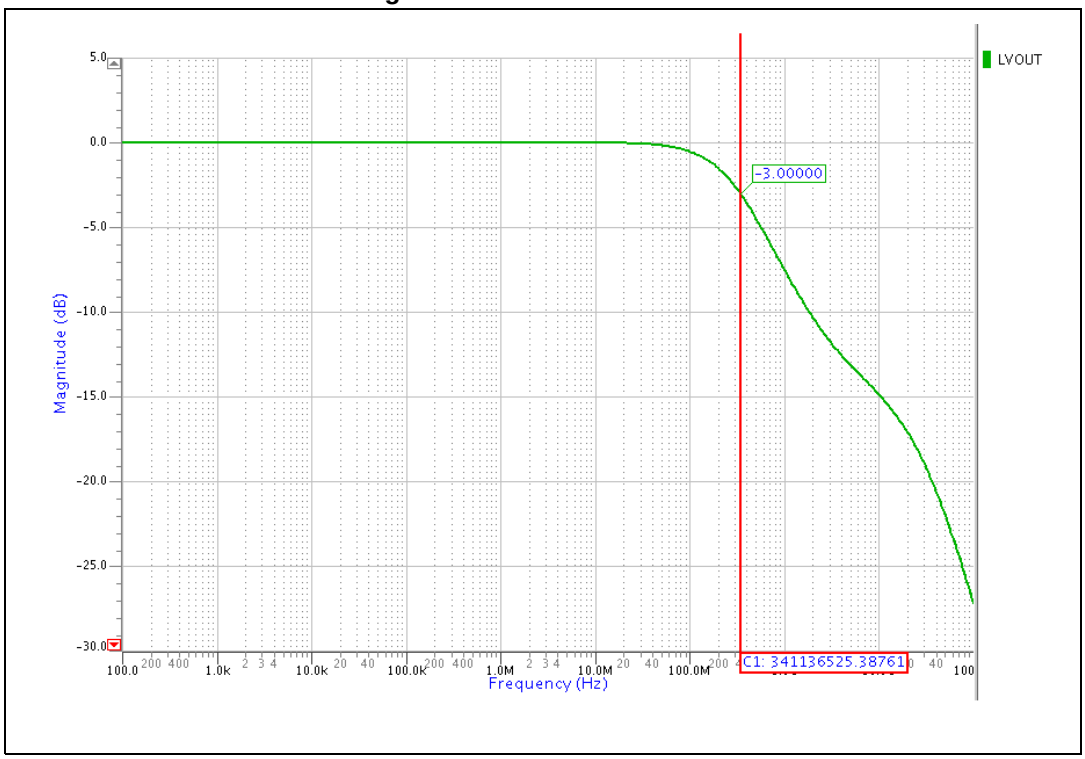
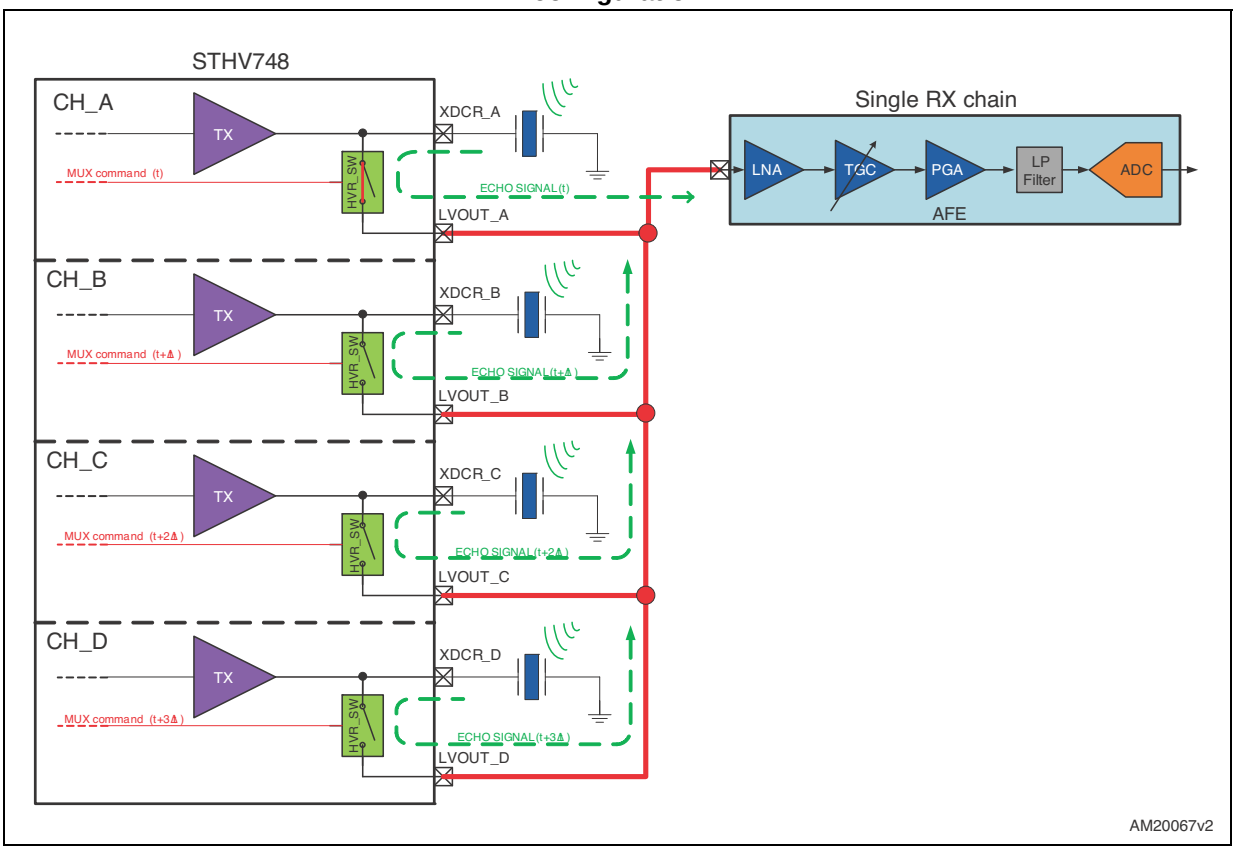


Figure 12. Possible external connection for LVOUT outputs with T/R SW in multiplexing driving configuration



9 Oscilloscope acquisitions

Figure 13. TX0 = ±60 V positive-negative pulses and immediately after TX1 = ±30 V positive-negative pulses, load 300 pF // 100 Ω

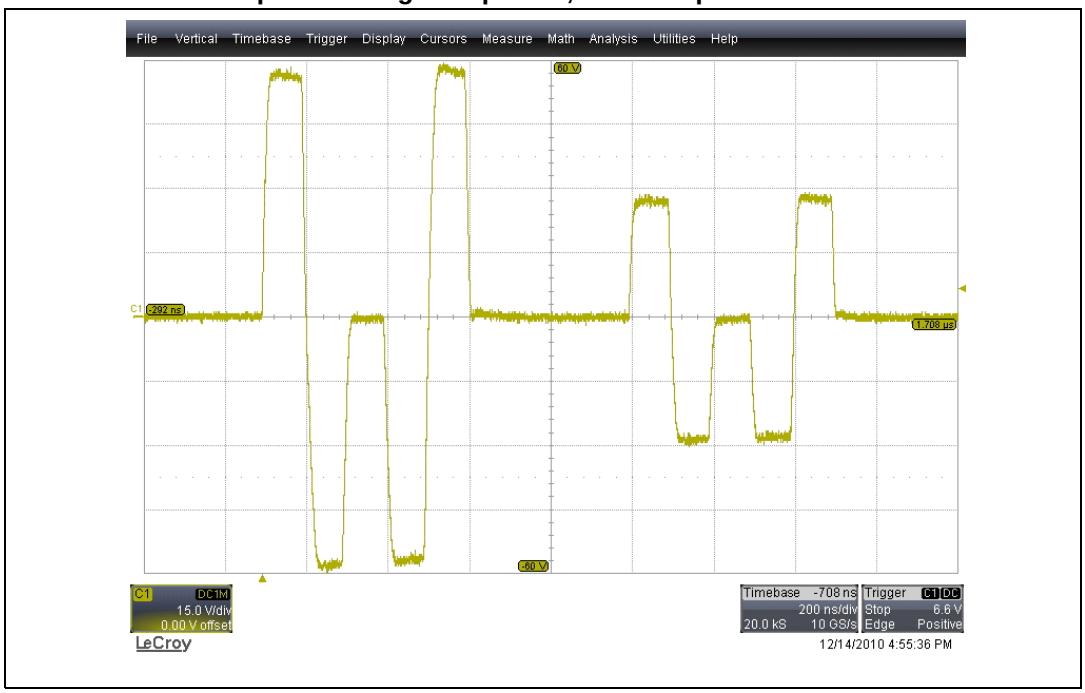


Figure 14. Five-levels HV output voltage

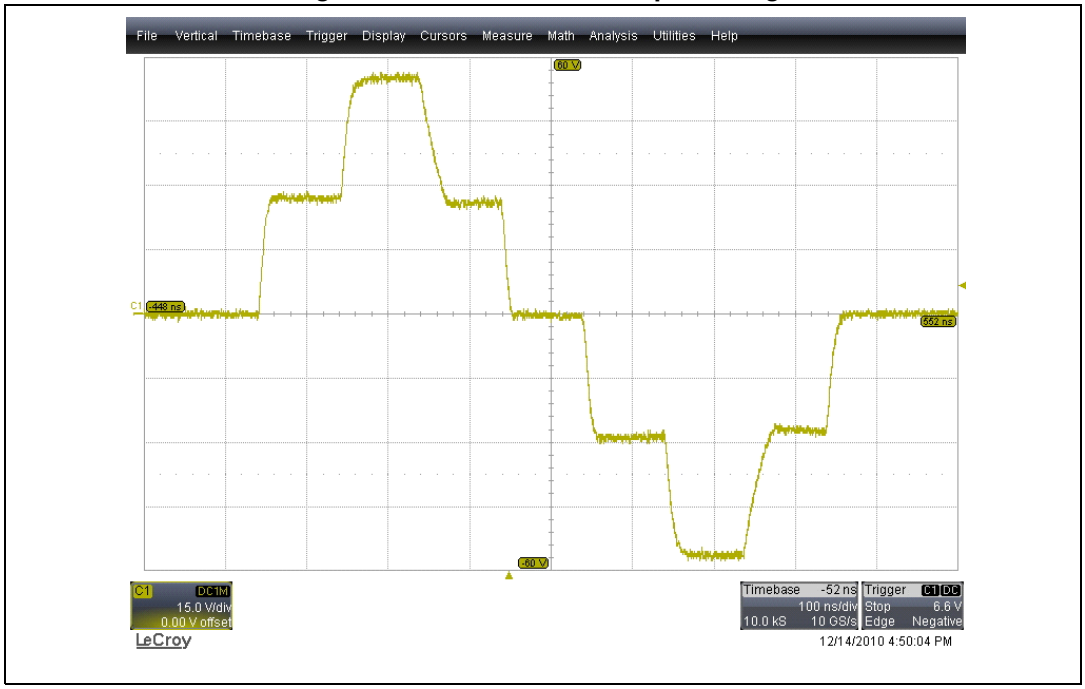


Figure 15. CW operations at 6 MHz

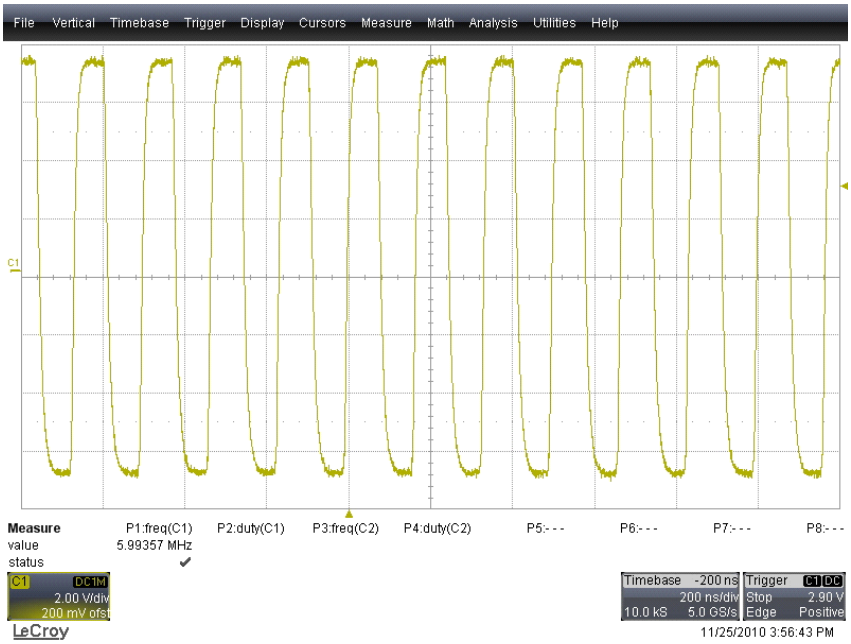


Figure 16. CW operations at 9 MHz

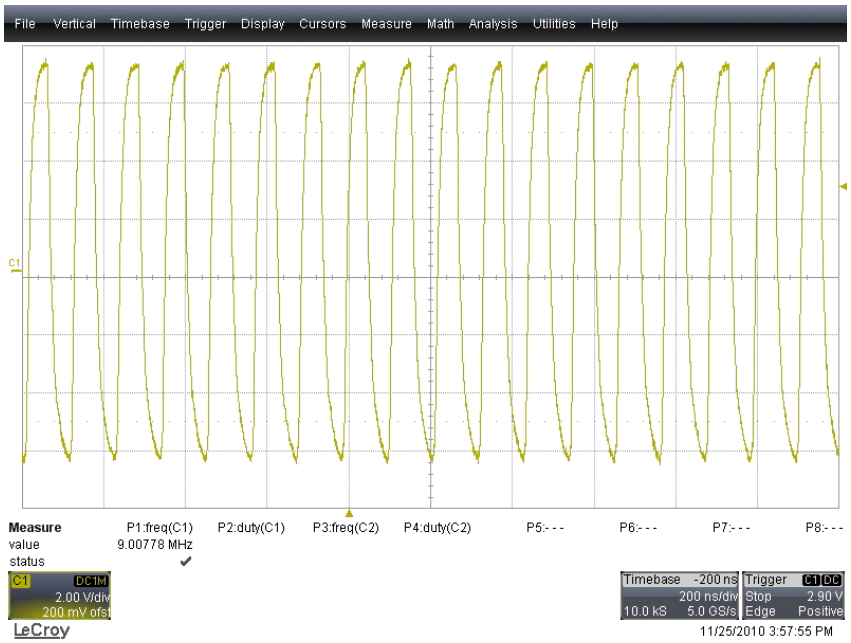
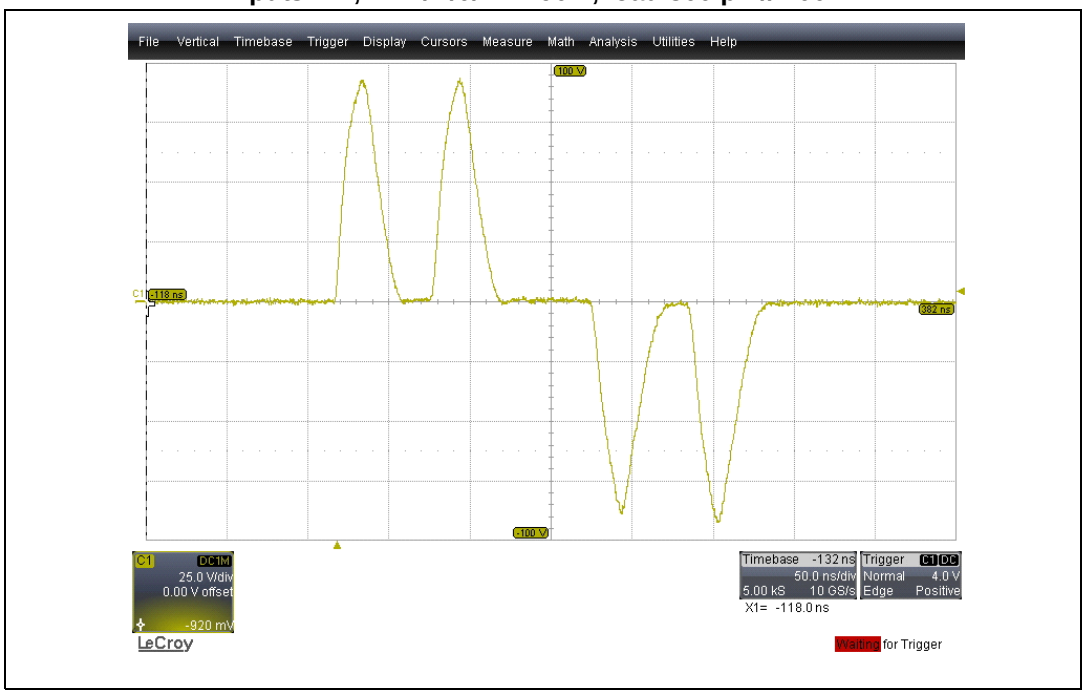


Figure 17. Two positive and two negative “short pulses” with 10 ns time width for inputs IN#, HVP/N/0/1 = ±90 V, load 300 pF // 100 Ω.



9.1 Output phase noise measurement in CW mode

9.1.1 Typical performance characteristics

Unless otherwise stated, the following conditions apply:

VDDP = +3.3 V, VDDM = -3.3 V, DVDD = +3.3 V, Exp-PAD = -5 V, HVP = +5 V, HVM = -5 V, no load, F_{in}= 5 MHz, T_A = 25 °C.

Figure 18. Measurement setup - CK1 = 640 MHz; CK2 = 5 MHz

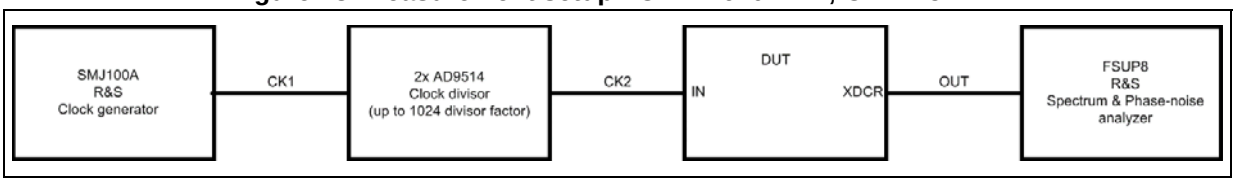
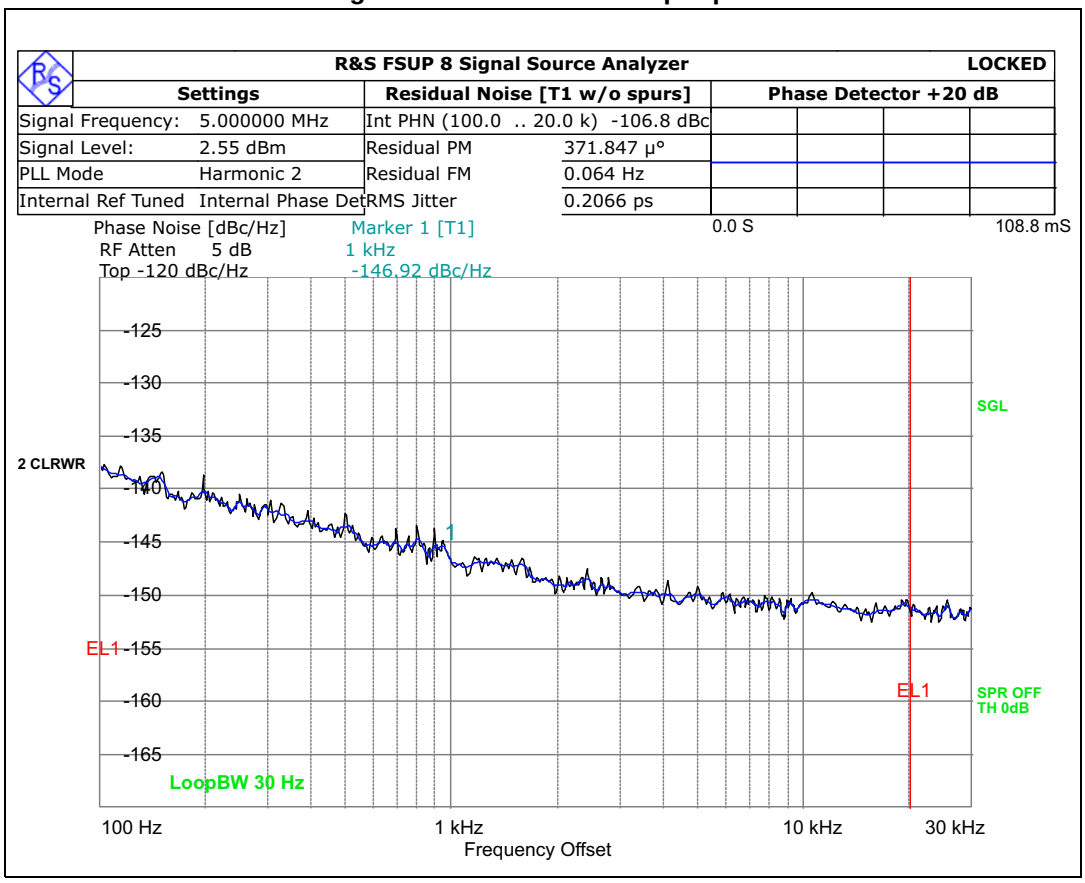


Figure 19. Phase noise output plot



Significant results from the output have been extracted[(a)]:

- Phase noise @1 kHz: -147 dBc/Hz
- RMS jitter [BW 100 Hz - 20 KHz]: 205 fs

a. Values measured leave room for improvement. As such, they are affected by a non-optimized setup.

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 QFN64 9 x 9 x 1.0 mm 64 pitch 0.50 package information

Figure 20. QFN64 9 x 9 x 1.0 mm 64 pitch 0.50 package outline

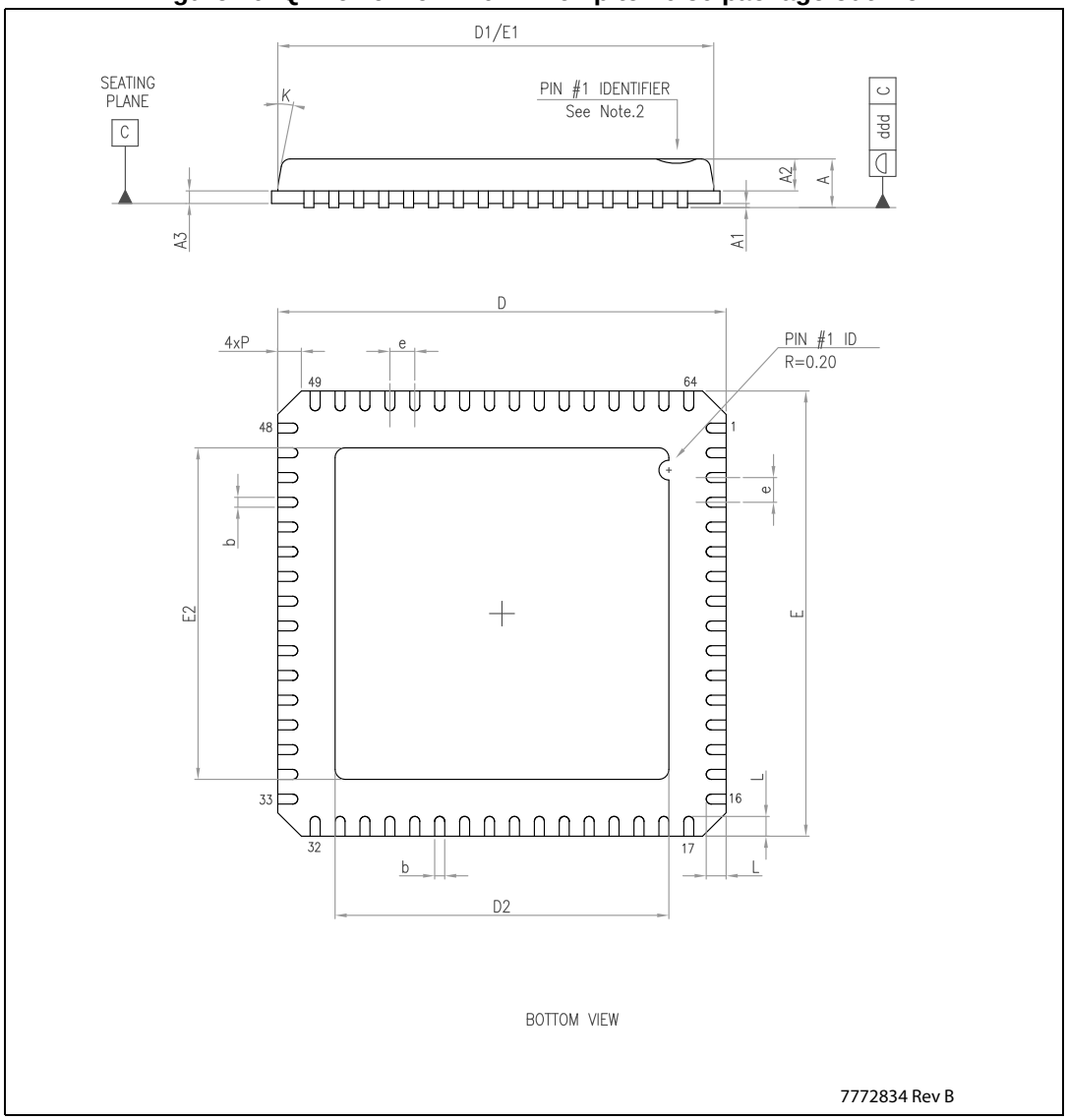


Table 11. QFN64 9 x 9 x 1.0 mm 64 pitch 0.50 package mechanical data

Dim	Min.	Typ.	Max.
A	0.8	0.9	1
A1		0.02	0.05
A2		0.65	1
A3		0.2	
b	0.18	0.25	0.3
D	8.85	9	9.15
D1		8.75	
D2	See exposed pad variation		
E	8.85	9	9.15
E1		8.75	
E2	See exposed pad variation		
e		0.5	
L	0.35	0.4	0.45
P			0.6
K			12
ddd			0.08

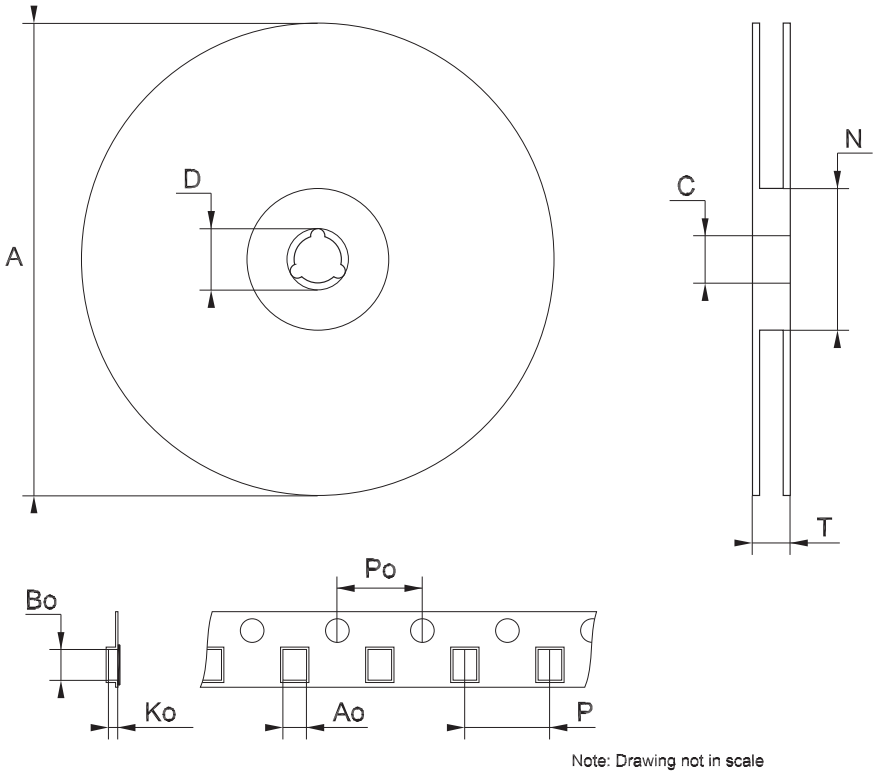
Table 12. Exposed-pad variation

Variation	6D2			E2		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.1	4.25	4.4	4.1	4.25	4.4
B	4.55	4.7	4.85	4.55	4.7	4.85
C	6.95	7.1	7.25	6.95	7.1	7.25
D	7.15	7.3	7.45	7.15	7.3	7.45

Note: QFN64 used for STHV748 has D variation option.

Figure 21. QFN64 9 x 9 x 1.0 mm 64 tape and reel information

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.196
Ao	12.25		12.45	0482		0.490
Bo	12.25		12.45	0482		0.490
Ko	2.1		2.3	0.083		0.091
Po	3.9		4.1	0.153		0.161
P	15.9		16.1	0.626		0.639



11 Revision history

Table 13. Document revision history

Date	Revision	Changes
20-Jan-2010	1	Initial release.
17-Feb-2010	2	Updated typo on coverpage.
09-Nov-2011	3	Updated *Table 6: Supply voltages and average currents*, *Table 9: Static electrical characteristics* and *Table 10: AC electrical characteristics*. Minor text changes.
11-May-2012	4	Updated the entire *Table 6: Supply voltages and average currents* title included. Updated title in *Figure 6: PW example 5 periods, HVP0 = 90 V, HVM0 = -90 V, T=200 ns, T_tx=1.2 µs, T_w=200 µs*. Minor text changes.
20-Jan-2016	5	– Updated *Features* on the coverpage and output jitter data in *Table 10*. – Added *Section 9.1: Output phase noise measurement in CW mode*. – Reformatted *Package information* section to current standards. – Minor text changes throughout the document.