AC108 Datasheet

4 Channel High Performance Voice Capture ADCs with I2C/I2S

Revision 1.1

July, 30, 2017

REVISION HISTORY

Revision	Data	Author	Description
V0.1	May,05,2016		Initial Version
V0.8	Mar,27,2017		Complete Version 0.8
V0.9	July,14,2017		Complete Version 0.9
V1.0	July,28,2017		Version 1.0
V1.1	July,30,2017		Change Power consumption data

DECLARATION

X-POWERS CANNOT ASSUME RESPONSIBILITY FOR USE OF ANY CIRCUITRY OTHER THAN CIRCUITRY ENTIRELY EMBODIED IN AN X-POWERS PRODUCT. NO CIRCUIT PATENT LICENSES, COPYRIGHTS, OR OTHER INTELLECTUAL PROPERTY RIGHTS ARE IMPLIED. X-POWERS RESERVES THE RIGHT TO MAKE CHANGES TO THE SPECIFICATIONS AND PRODUCTS AT ANY TIME WITHOUT NOTICE.

CONTENTS

4 Channel Voice Capture ADCs IC

FEATURES

■ ADC future

- 108 dB dynamic range (A-weighted) @ 0 dB boost gain
- –90 dB THD+N @ 0 dB boost and 1.4Vpp input
- 4 programmable boost amplifiers with 0dB to 30dB in 1dB step
- ADC sample rates supported: 8kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz,96KHz
- Analog and digital mixer in record data path

■ Analog Input and output

- Four fully differential microphone inputs: MIC1P/N ~MIC4P/N
  - -Can be configured as pseudo differential, single-ended mode
- Four low noise mic bias outputs: MIC1_BIAS~MIC4_BIAS
  - -Programmable bias voltage 1.5V to 3.4V
  - -4uV noise level in signal bandwidth

■ Digital Output

- Two digital microphone SCLK output@1M~3M
- Two I2S data output:
  - - I2S/PCM format using 2 pins to output 4 channel data
  - -TDM format using 1 pin to output 4 channel data even 16 channel of 4 devices
  - -Encoding format using 1 pin to output 4 channel data even 16 channel of 4 devices

■ Other Features

- PLL support a wide input for wide range
- Integrated LDO allowing single supply (3.3V~5V)
- 4 ADC channel 16mA@3.3V for low power consumption application
- TWI control interface support up to 400 kHz
- QFN 48-pin package, 6mm x 6mm

DESCRIPTION

The AC108 is a highly integrated quad-channel ADC with I2S/TDM output transition. It's designed for multi-microphone array in high definition voice capture and recognition application platforms.

The integrated digital PLL supports a large range of input/output frequencies, and it can generate required system clocks from common reference clock such as 6-/12-MHz, 6.144-/12.288-MHz, 5.6448-/11.2896-MHz, 13MHz and 19.2MHz. The audio sample 8kHz, 12kHz,16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 96kHz is supported.

The AC108 integrates four synchronized ADCs with independent programmable mic bias voltage and mic boost amplifier to deliver valid channel data that channel crosstalk can be eliminated. The analog input port MIC1P/N ~MIC4P/N is designed as four differential microphone pin or single-ended line-in pin .Two smart digital mic interfaces are supported to make low jitter clock output and decimation filter for up to four digital mic. Independent digital voice controllers are provided in each channel.

The AC108 can transit its four channels output data over two I2S ports by standard I2S or PCM format, also a single port by TDM format. A new format called encoding mode can also be used to transit four channel data when the I2S format of AP is normal protocol types. Furthermore, one to four device can be combined to transit up to 16 channels output data by a single TDM line.

The device includes several DSP features such as high-pass filter, mixer, and volume control.

AC108 is controlled through TWI (2-wire serial interface). The clock supports up to 400 KHz rate. It works only in the slave mode.

APPLICATIONS

- Smart Voice Assistant Systems
- Voice Recorders
- Digital Cameras and video cameras
- Voice Conferencing System

FUNCTIONAL BLOCK DIAGRAM

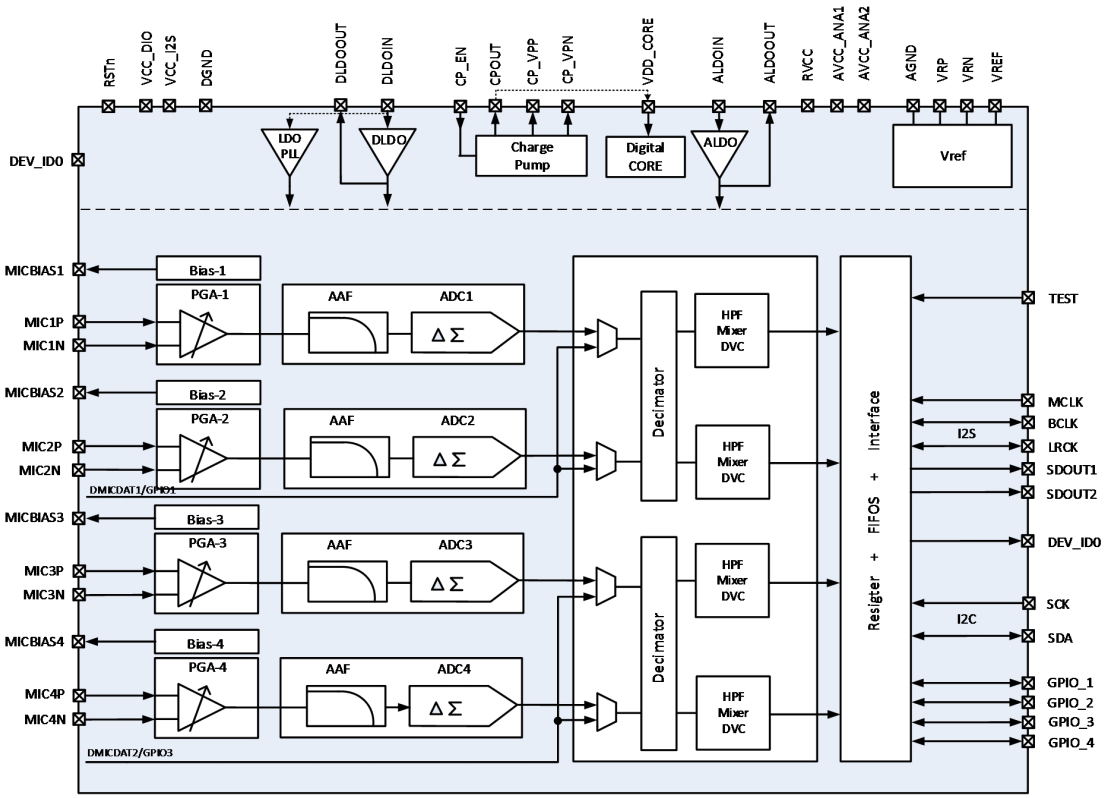


Figure 1 Functional Block Diagram

PIN ASSIGNMENT

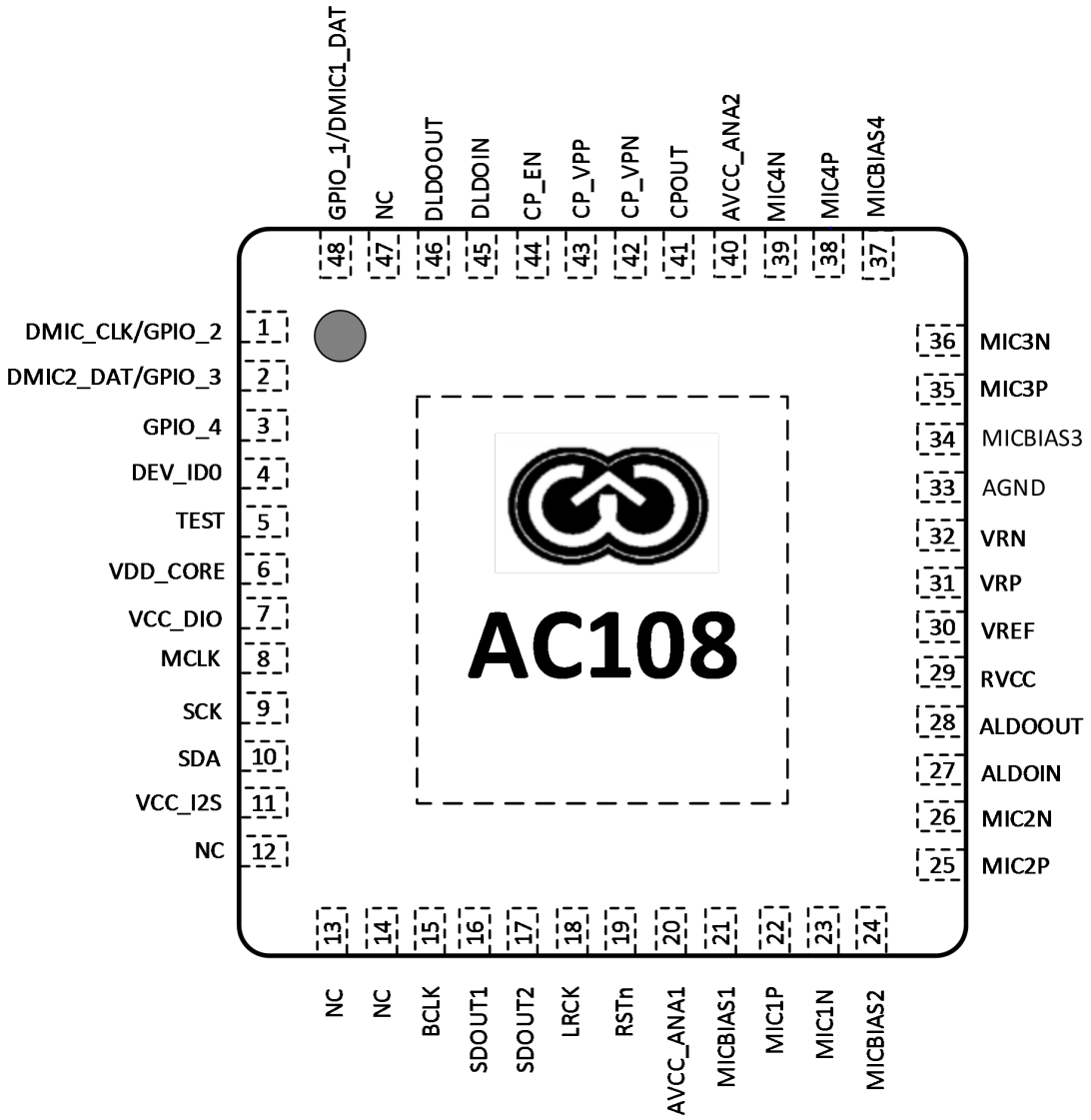
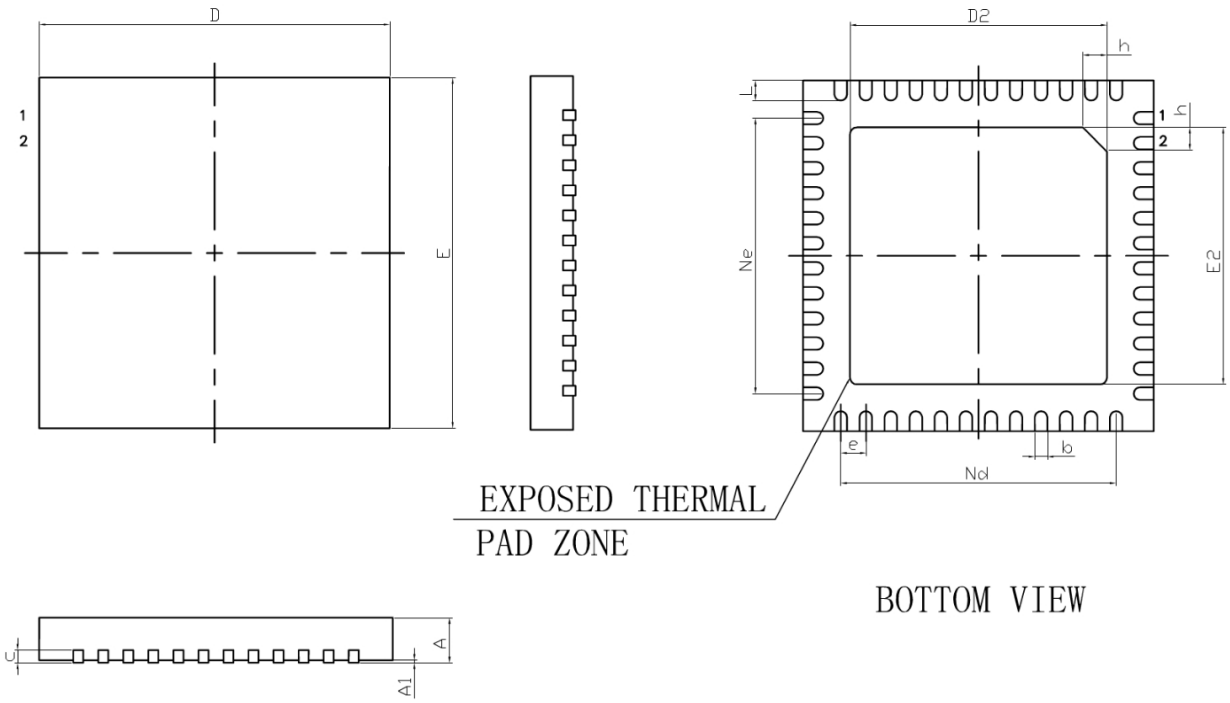


Figure 2 Pin Assignment

PACKAGE DIMENSION



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0.75	0. 80
A1	—	0.02	0. 05
b	0. 15	0.20	0. 25
c	0. 18	0.20	0. 23
D	5. 90	6. 00	6. 10
D2	4. 10	4.20	4. 30
e	0. 40BSC		
Ne	4. 40BSC		
Nd	4. 40BSC		
E	5. 90	6. 00	6. 10
E2	4. 10	4.20	4. 30
L	0. 35	0.40	0. 45
h	0. 30	0. 35	0. 40
L/F载体尺寸 (MIL)	177*177		

Figure 3 Package Dimension

PIN/SIGNAL DESCRIPTION

This chapter describes the 48 pins of AC108 from four aspects: pin number, signal name, type, and pin definition. All the pins are classified into four groups, including digital IO pin, analog IO pin, filter/reference, and power/ground.

There are five pin types here: O for output, I for input, I/O for input/output, P for power, and G for ground.

Pin Number	Signal Name	Type	Description
Digital IO Pins			
8	MCLK	I	I2S interface master input clock 1
15	BCLK	I/O	I2S interface serial bit clock
16	SDOUT1	O	I2S interface serial data output 1
17	SDOUT2	O	I2S interface serial data output 2
18	LRCK	I/O	I2S interface synchronous clock
48	GPIO_1 DMICDAT1	I/O I	General purpose input output 1 Digital MIC stereo data1 input
1	GPIO_2 DMICCLK	I/O O	General purpose input output 2 Digital MIC CLK output
2	GPIO_3 DMICDAT2	I/O I	General purpose input output 3 Digital MIC stereo data2 input
3	GPIO_4	I/O	General purpose input output 4
9	SCK	I	TWI interface serial clock input
10	SDA	I/O	TWI interface serial data(Open-drain)
4	DEV_ID0	I	TWI interface device ID control
19	RSTn	I	Chip rest pin
5	Test	I	Scan test for QAQC
Analog IO Pin			
21	MICBIAS1	O	Bias voltage output for MIC1
22	MIC1P	I	Positive differential input for MIC1
23	MIC1N	I	Negative differential input for MIC1
24	MICBIAS2	O	Bias voltage output for MIC2
25	MIC2P	I	Positive differential input for MIC2
26	MIC2N	I	Negative differential input for MIC2
34	MICBIAS3	O	Bias voltage output for MIC3
35	MIC3P	I	Analog Positive differential input for MIC3
36	MIC3N	I	Negative differential input for MIC3
37	MICBIAS4	O	Bias voltage output for MIC4
38	MIC4P	I	Positive differential input for MIC4
39	MIC4N	I	Negative differential input for MIC4
44	CP_EN	I	The charge pump enable
Filter/Reference			
29	CP_VPP	I/O	Charge pump flying-back capacitor positive terminal
31	CP_VPN	I/O	Charge pump flying-back capacitor negative terminal
30	VREF	O	Internal reference voltage
31	VRP	O	Internal reference voltage
32	VRN	O	Internal reference voltage

Power/Ground			
45	DLDOIN	P	The digital LDO Power input
46	DLDOOUT	P	The LDO Power output 3.3V for digital part
41	CPOUT	P	Charge pump output 1.2V for digital core
27	ALDOIN	P	The analog LDO Power input
28	ALDOOUT	P	The LDO Power output 3.3V for analog part
29	RVCC	P	Analog power for internal reference
20	AVCC_ANA1	P	Analog power for ADC1&2 and PGA1&2
40	AVCC_ANA2	P	Analog power for ADC3&4 and PGA3&4
6	VDD_CORE	P	Digital core power
7	VCC_DIO	P	Digital power for digital I/O buffer (GPIO&TWI&MCLK)
11	VCC_I2S	P	Digital power for digital I/O buffer (I2S&RSTn)
33	AGND	G	Analog ground
49	GND	G	Digital ground
Others			
12,13,14,47	NC	--	Not connected

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

Symbol	Parameter	MIN	MAX	Unit
DLDOIN	LDO Input power for digital 3.3V domain cell control	-0.4	5.5	V
ALDOIN	LDO Input power for analog part	-0.4	5.5	V
VDD_CORE	Digital power for Audio digital core, it can be generate by inner CP	-0.3	1.32	V
VCC_DIO	Digital power for digital I/O buffer	-0.3	3.63	V
VCC_I2S	Digital power for digital I/O buffer	-0.3	3.63	V
T_A	Operating Ambient Temperature	-40	85	℃
V_{ESD}	ESD	4	--	KV

Recommended Operating Conditions

Parameter	Description	MIN	TPY	MAX	Unit
DLDOIN	LDO Input power for digital 3.3V domain cell control	3.15	3.3/5	5.25	V
ALDOIN	LDO Input power for analog part	3.15	3.3/5	5.25	V
VDD_CORE	Digital power for Audio digital core, it can be generate by inner LDO	1.08	1.2	1.32	V
VCC_DIO	Digital power for digital I/O buffer	--	1.8/3.3	3.63	V
VCC_I2S	Digital power for digital I/O buffer	--	1.8/3.3	3.63	V
GND,AGND	Ground reference	--	0	--	V

Static Characteristics

Symbol	Parameter	Test condition	Min	Typical	Max	Units
V_{IN}	Input Voltage Range	--	-0.3	--	VCC_DIO+0.3 VCC_I2S+0.3	V
V_{IH}	High Level Input Voltage	VCC_DIO=3.3V VCC_I2S=3.3V	2.4	--	3.6	V
		VCC_DIO=1.8V VCC_I2S=1.8V	1.4	--	1.98	
V_{IL}	Low Level Input Voltage	VCC_DIO=3.3V VCC_I2S=3.3V	-0.3	--	0.7	V
		VCC_DIO=1.8V VCC_I2S=1.8V	-0.3	--	0.7	
V_{OH}	High Level Input Voltage	VCC_DIO=3.3V VCC_I2S=3.3V	2.7	--	NA	V
		VCC_DIO=1.8V VCC_I2S=1.8V	1.5	--	NA	
V_{OL}	Low Level Input Voltage	VCC_DIO=3.3V VCC_I2S=3.3V	NA	--	0.4	V
		VCC_DIO=1.8V	NA	--	0.4	

		VCC_I2S=1.8V				
C_{IN}	Input Capacitance	--	NA	NA	5	pF
C_{OUT}	Output Capacitance	--	NA	NA	5	pF

ANALOG PERFORMANCE CHARACTERISTICS

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UINT
ADC Input Path Performance	**MIC1 /2/3/4 via ADC to I2S DLDOIN=ALDOIN=5.0V, VCC_I2S=VCC_DIO=3.3V**					
	DR(A-weighted)	PGA=0 dB		108		dB
	THD+N			-90		dB
	DR(A-weighted)	PGA=12 dB		106		dB
	THD+N			-84		dB
	DR(A-weighted)	PGA=24 dB		100		dB
	THD+N			-83		dB
	DR(A-weighted)	PGA=30 dB		95		dB
	THD+N			-83		dB
	Crosstalk（L/R）	10mV，1KHz，30dB Gain		90		dB
ADC Input Path Performance	**MICBIAS1 /2/3/4 without bypass capacitor DLDOIN=ALDOIN=5.0V, VCC_I2S=VCC_DIO=3.3V**					
	Output Scale		1.5	2.1	3.4	V
	Bias Current			4		mA
	Noise Level		1.7	4		uV

TYPICAL POWER CONSUMPTION

Default Test Conditions:

DLDOIN=ALDOIN=5V, DLDO Bypass, VCC-DIO=VCC-I2S=3.3V

OPERATING MODE	DLDO	ALDO	Charge Pump	VREF	VDD-DIO	VDD-I2S	Total
Standby							
DLDO enabled	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	170uA
1- ADC record on high performance mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	8.2mA
2- ADC record on high performance mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	15mA
4- ADC record on high performance mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	28mA
1- ADC record on low power mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	5.5mA
2- ADC record on low power mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	9.3mA
4- ADC record on low power mode							
Charge Pump enabled Analog LDO enabled I/O enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	16.5mA

TYPICAL APPLICATION DIAGRAM

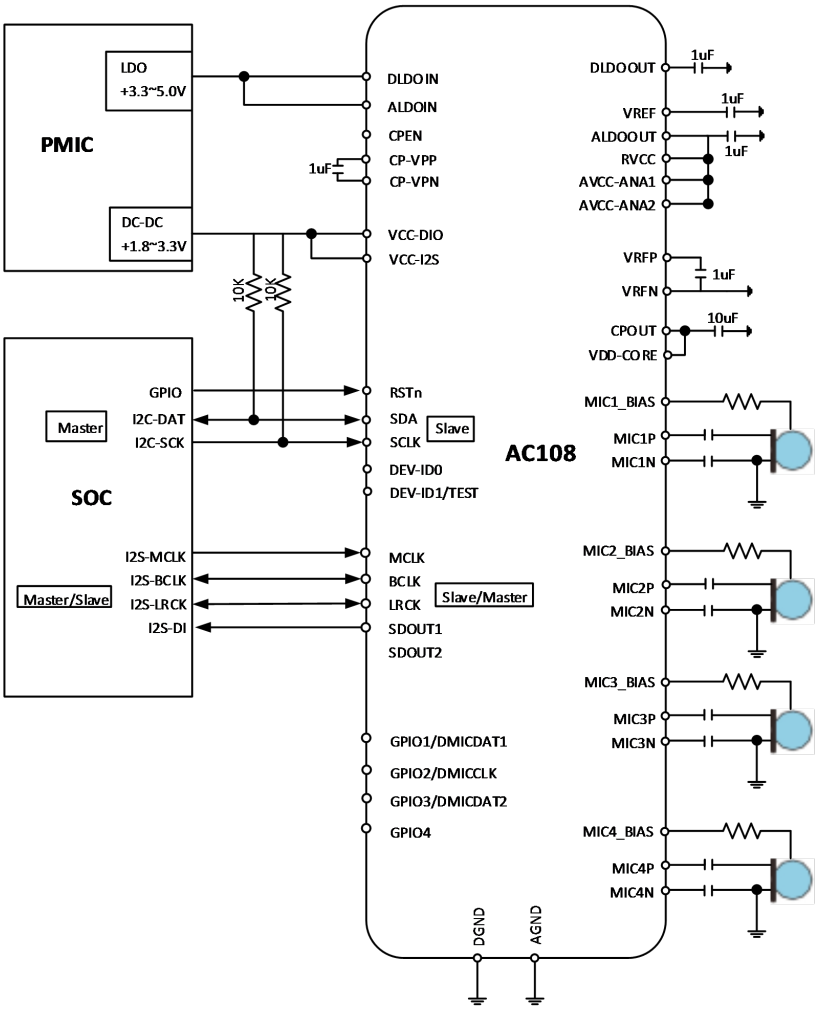


Figure 4 Typical Application Diagram